Novel Cell based on Reduced Single-phase Active Front End for Multicell Converters.

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Abstract— **Multilevel converters are a very interesting alternative for medium and high power drives. One of the more flexible topologies of this type is the Multicell converter.**

This paper presents a new regenerative cell suitable for cascaded multilevel inverters. The cell uses a reduced single-phase active rectifier at the input and an H-bridge inverter at the output side. The cell has a reduced switch count and presents a very good performance, controlling effectively the waveform of the input current and of the output voltage.

The results presented in this paper confirm that this medium voltage inverter effectively eliminates low frequency input current harmonics at primary side of the transformer and operates without problem in regenerative mode.

I. Introduction

In the last years, the necessity of increase the power level on industry, has sustained the continuous development of Multilevel converters due to their capability of handling voltages up to 6.9[kV] and power of several Megawatts. Among different topologies [1], the cascaded Multicell [2] inverter has received an important attention .

The original converter proposed in [2] uses cells with diode rectifiers that does not allow to transfer power from the load to the power supply (regeneration). Several loads, like laminators and downhill conveyors demand regeneration capability on the converter. This fact has motivated several researchers to seek for alternatives of cascaded topologies with regeneration capability, which can be done by replacing the diode bridge with a PWM active rectifier at the input side obtaining regenerative cells [3],[4].

The first part of this paper presents a general Multicell converter and a review of different regenerative cells with their corresponding advantages and drawbacks, considering the number of switches, control issues and their overall performance. In Section III a new cell topology is introduced based on a half-bridge PWM rectifier and a three-level single phase inverter (H-bridge). A standard control scheme is used [5], [6] and some modifications are included in order to guarantee a very high input power factor and prevent the voltage imbalance on the capacitors. A multicell converter using the proposed regenerative cell is presented in Section IV and a special interconnection among the input transformers is used in order to ensure the cancellation of low order harmonics.

Results for a 7-level converter using the proposed cell are included in Section V, showing a good quality output signals, while working with a very high input power factor in rectifying and regenerative mode.

II. Multicell Converter

The Multicell converter was introduced by Hammond [2]; this topology is based in the series connection of units known as *cells* for each output phase, as shown in Fig. 1.

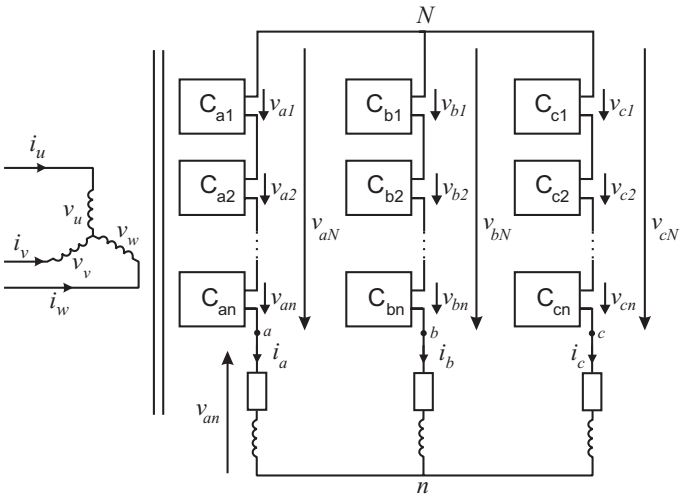

Fig. 1. Control scheme of the proposed cell.

Each cell is a structure based on a rectifier fed by an isolated voltage source, a capacitive DC-link and an inverter structure. The series connection of the inverters of the cells produces a multilevel voltage (v_{xN} $x = a, b, c$), which corresponds to the addition of the output voltage of each cell:

$$v_{xN} = \sum_{y=1}^{n} v_{xy} \quad , \; x = a, b, c \tag{1}$$

The cell structure proposed in [2] is based on a three-phase diode bridge, one DC-link capacitor and a single-phase three-level inverter (or *H-bridge*) as shown in Fig. 2-a). This topology needs a complex input transformer in order to reduce the low order harmonics and, due to the diode bridge, cannot reverse the power flux from the load to the supply.

In [3] the authors propose the use of PWM rectifiers as the front-end of the cells for applications that require

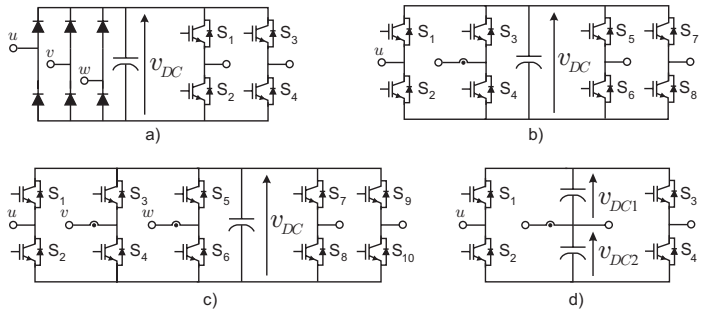

Fig. 2. Cell topologies: a) Non-Regenerative; Regenerative with: b) Single-phase PWM Rectifier; c) Three-phase PWM Rectifier; d) Reduced number of semiconductors.

regeneration capability, and a single-phase PWM-rectifier like the one shown in Fig. 2-b) is used. This cell, known as H-H cell, requires a simpler transformer than the one shown in Fig. 2-a) and can reach a very high power factor at the input with a proper input transformer connection. The main drawbacks of this cell is that the DC-link presents ripple at the double of input voltage frequency ($2f_s$), and the input current can not be controlled in rotating frame, so PI controllers are not recommended [7].

The cell presented in [4] uses a three-phase PWM rectifier as shown in Fig. 2-c), this cell requires ten semiconductors, an extra current sensor and a more complex transformer, but does not present pulsating power, even, the DC-link capacitor can be reduced if extra input current harmonics are included in order to cancel the pulsating power from the H-bridge inverter. Another important advantage is that the currents can be controlled in *dq* rotating frame.

The cell shown in Fig. 2-d) is presented in [8], this cell requires only four semiconductors, two for rectifier stage and two for the inverter stage and two DC-link capacitors. The main issues of this cell are:

i. An extra balance control must be included in order to keep both DC-link voltages (v_{DC1} and v_{DC2}) at the same level, that implies that two DC-link voltage sensors are required.

ii. The output voltage of this cell has only two levels.

iii. Use the same simple input transformer used for the cell of Fig. 2-b).

III. Proposed Cell

A. Topology Description.

The proposed cell is shown in fig. 3. This cell only requires two power semiconductors for the rectification stage, and four for the classic H-bridge, so the complete cell can be implemented in a three-phase inverter module.

A.1 Rectifier operation.

From Fig. 3 it is easy to see that T_1 and T_2 must work in complementary mode, otherwise, the DC-link would be short-circuited, or the input inductance L would be open-circuited. So just two conduction possibilities are allowed for the rectifier: $T_1 = 1$, $T_2 = 0$ or $T_1 = 0$, $T_2 = 1$. Both

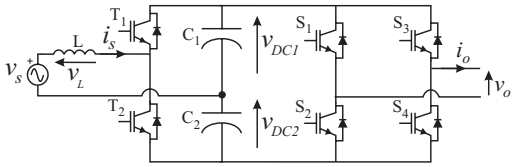

Fig. 3. Power circuit of the proposed cell.

conduction states are shown in fig. 4-a) and -b) respectively, where the Z impedance represents the effect of the H-bridge inverter.

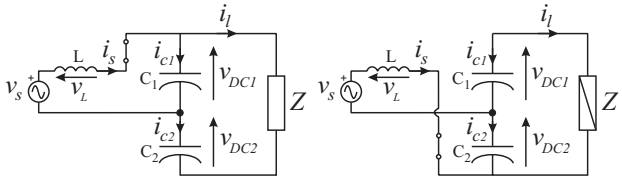

Fig. 4. Rectifier behavior when: a) T_1=1; b) T_2=1.

Note that for a correct operation it is assumed that the DC-link voltage on each capacitor is always greater than the input voltage v_s. Under this assumption the following expression can be obtained:

a)$T_1 = 1$:

From fig. 4-a) it can be seen that:

$$v_L = L\frac{di_s}{dt} = v_s - v_{DC1} \tag{2}$$

As $v_{DC1} > v_s$, (2) implies that v_L is always negative, so i_s decreases its value. On the other hand, the capacitor currents are:

$$i_{c1} = i_s - i_l \tag{3}$$

$$i_{c2} = -i_l \tag{4}$$

and

$$v_{DC1} = \frac{1}{C_1}\int i_{c1}(\tau)\, d\tau \tag{5}$$

$$v_{DC2} = \frac{1}{C_2}\int i_{c2}(\tau)\, d\tau \tag{6}$$

if $i_s > 0$ C_1 will be charged by the mains, otherwise, if $i_s < 0$, the voltage in C_1 will decrease its value. The voltage in C_2 will depends exclusively on the load condition.

b)$T_1 = 0$:

As seen in fig. 4-b), if $T_1 = 0$, (2) changes to:

$$v_L = L\frac{di_s}{dt} = v_s + v_{DC2} \tag{7}$$

due to $v_{DC2} > v_s$, $v_L > 0$ so i_s increases its value.

Under this condition, (3) and (4) change to:

$$i_{c1} = -i_l \tag{8}$$

$$i_{c2} = -i_s - i_l \tag{9}$$

If $i_s > 0$ the capacitor C_2 will be discharged, otherwise, if $i_s < 0$, the voltage in C_2 will increase its value. As in

the previous section, the voltage in C_1 depends on the load condition.

The control scheme must adjust the duty cycle in order to keep the voltages v_{DC1} and v_{DC2} at its reference value.

A.2 Inverter Unit

Fig. 5 shows the four conduction states for an H-bridge inverter. Note that this topology generates up to three different output voltage levels based on the full DC-link voltage $v_{DC} = v_{DC1}+v_{DC2}$, disregarding the rectifier topology.

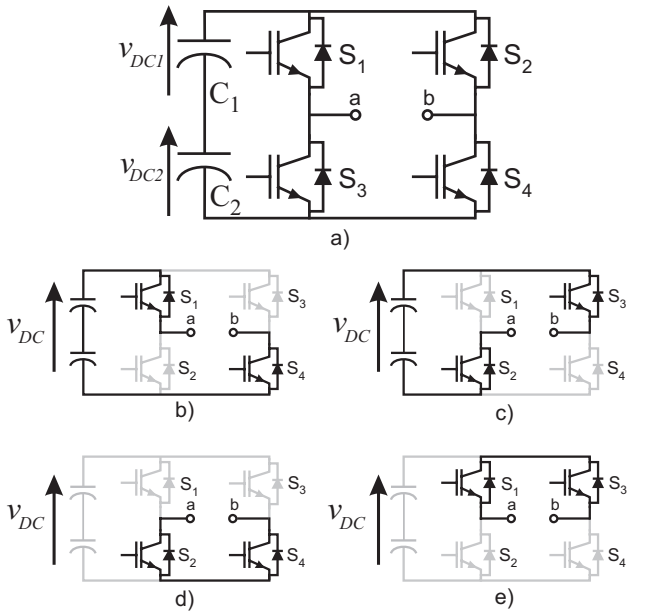

Fig. 5. a) H-bridge inverter. Output voltage b)$v_{ab} = v_{DC}$; c)$v_{ab} = -v_{DC}$; d) and e)$v_{ab} = 0$

B. Control Scheme

The control scheme for the rectifier side of this Semireduced cell is shown in Fig. 6. This scheme uses a voltage controller C_v to keep the DC-link voltage v_{DC} constant and a current controller C_c that allows to achieve a high input power factor. Typically C_v and C_c are chosen as simple PI controllers. However, in this case a linear resonant controller at mains frequency $\omega_s = 2\pi f_s$ is proposed for C_c to provide perfect phase tracking on the current loop.

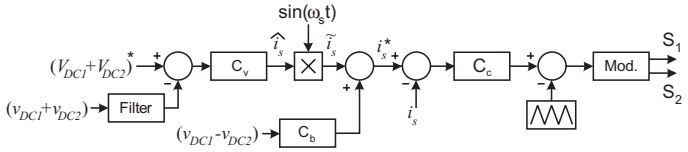

Fig. 6. Control scheme of the proposed cell.

Working with a sinusoidal input current of frequency f_s in phase with the input voltage implies that the instantaneous input power $p_i(t)$ has a pulsating component at $2\omega_s$:

$$p_i(t) = \hat{v}_s \sin(\omega_s t)\ \hat{i}_s \sin(\omega_s t) = \frac{\hat{v}_s \hat{i}_s}{2}\Big[1 - \cos(2\omega_s t)\Big] \quad (10)$$

so, the entire DC-link voltage v_{DC} presents a ripple at $2\omega_s$. As this ripple is a consequence of working with a high power factor it cannot be compensated, so it must be ignored by the voltage controller. For this reason a band-stop filter at $2\omega_s$ in the v_{DC} measurement is included.

Some research studies [6], [5] have discussed a voltage imbalance phenomenon between both capacitors. This studies are focused on a rectifier side identical to the one proposed on this paper but with a rather different inverter topology. According to these authors, the voltage imbalance is produced by several factors, including offset introduced by analog components, different initial conditions and asymmetry in both capacitances. This last factor is of particular interest in this case due to the usual imprecision in high voltage electrolytic capacitors.

The problem is solved by introducing a DC offset in the current reference for the current loop. As stated on the current literature, a simple proportional controller should be enough to compensate the imbalance. However, according to (3) and (9), it can be noticed that there is a strong component of frequency f_s[Hz] in both v_{DC1} and v_{DC2}. Since these components are shifted in 180^o, they appear as an amplified f_s[Hz] component on the imbalance $\Delta v = v_{DC1} - v_{DC2}$.

This component propagates through the P controller and, since $\tilde{i}_s(t)$ is nearly a f_s[Hz] AC current, modifies the current reference phase. Thus, the current loop will track $i_s^*(t)$ instead of $\tilde{i}_s(t)$, leading to an undesirable shifted phase input current that degrades the power factor.

A simple solution to this issue is achieved by introducing a notch filter on the Δv measurement. The notch filter should provide a considerable attenuation at f_s[Hz] in order to carry the input power power factor near unity. Comparison results using the traditional P controller method and the new proposed notch-P controller are shown in Fig. 7, demonstrating the effectiveness of the proposed scheme. Note that this results are obtained with a purely resistive load in order to override the effects of harmonic injection introduced by the H-bridge operation.

IV. Multicell Converter with the Proposed Cell.

Fig. 8 shows a 7-level Multicell converter using the proposed cell.

The input current on each cell presents several harmonics component due to H-bridge operation. This phenomenon is described, for an H-H cell, in [9]. In order to obtain a proper cancellation of these harmonics components on the primary side of the transformer, the interconnection proposed in [9] is used.

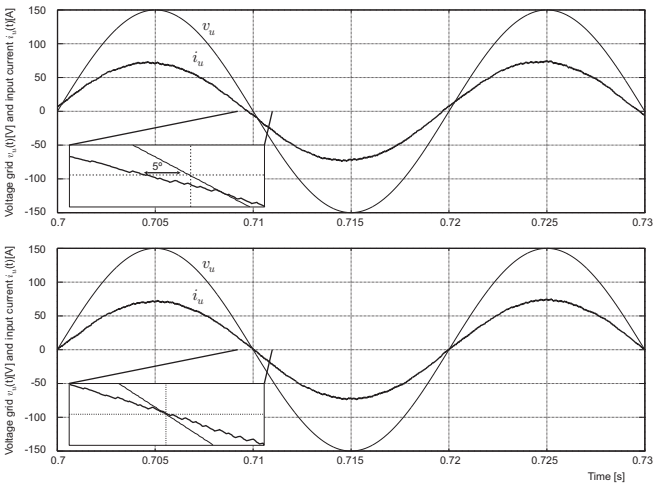

Fig. 7. Input current and grid voltage with: (a) P imbalance controller , (b) Notch-P imbalance controller.

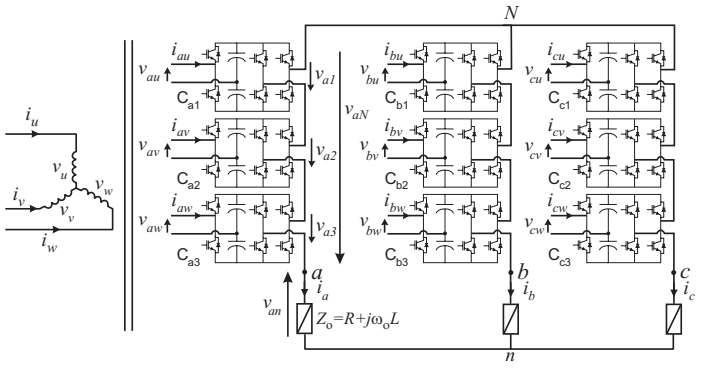

Fig. 8. 7-level Multicell converter with the proposed cell.

According to Fig. 8 the following relationships hold:

$$i_j = k(i_{aj} + i_{bj} + i_{cj}) \tag{11}$$

$$v_j = \frac{1}{k}v_{aj} = \frac{1}{k}v_{bj} = \frac{1}{k}v_{cj} \qquad ,j = u, v, w \tag{12}$$

where k represents the turns ratio of the input transformer. For simplicity in this paper it is assumed that $k = 1$.

V. Results

Results of the converter in Fig. 8 using the proposed power cell in Fig. 3 are presented using a 150[V]-50[Hz] grid with an input impedance of $Z_s = 0.8 + j\omega_s 0.0058$ on each cell, and in the output side a frequency of $f_o = 20$[Hz] and an impedance of $Z_o = 150 + j\omega_o 0.03$.

Fig. 9 shows the input current of cell C_{a1} and the resulting current at the primary side of the input transformer. Clearly, the interconnection between the cells allows the cancellation of the low frequency harmonics in steady state, leading to a highly sinusoidal input current. Note that Fig. 9-b) shows that the high frequency ripple is also reduced in the primary current by an appropriate shift of the carrier signals of each cell.

This cancellation in the input current waveform is confirmed by the frequency spectra shown in Fig. 10. The voltage imbalance suppression is ratified by the results of Fig. 11. Note that according to Fig. 12 the 50 [Hz] components in both v_{DC1} and v_{DC2} are cancelled in v_{DC} due to the 180^o phase shift between them.

The waveform in Fig. 13-a) exposes the 7 level output voltage generated by the proposed converter due to the cell interconnection. This voltage generates a very sinusoidal load current that can be seen in Fig. 13-b).

The regenerative capability of the converter is demonstrated by the results of Fig. 14. Extracting power from the load temporarily increases the DC-link voltage v_{DC} of the cells as shown in Fig. 14-a), forcing the current loop of each cell to invert the phase of its input current. Fig. 14-b) shows the primary side input current during transient, which preserves unity power factor on rectifying and regeneration conditions.

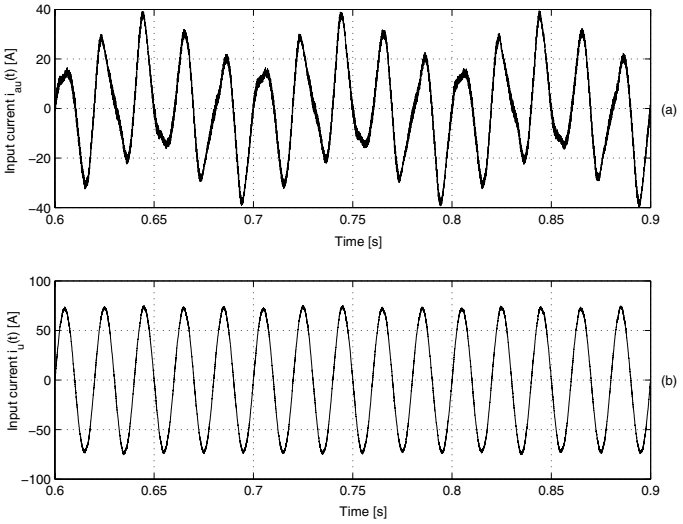

Fig. 9. (a) Single cell input current $i_{au}(t)$, (b) converter input current $i_u(t)$.

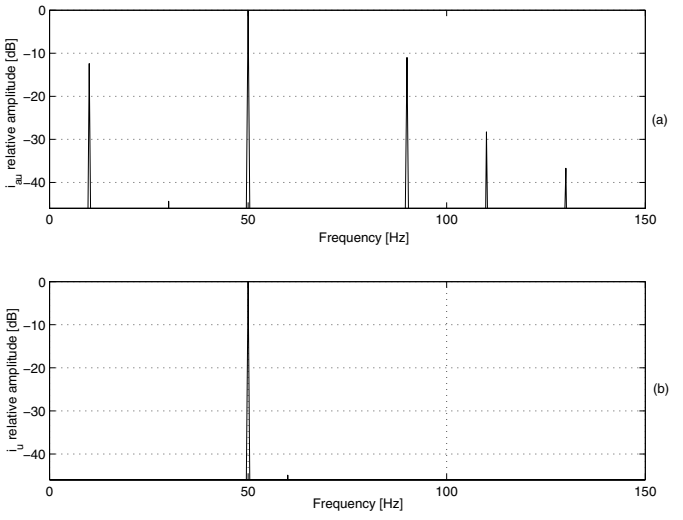

Fig. 10. Frequency spectra of input currents: (a) $i_{au}(t)$, (b) $i_u(t)$.

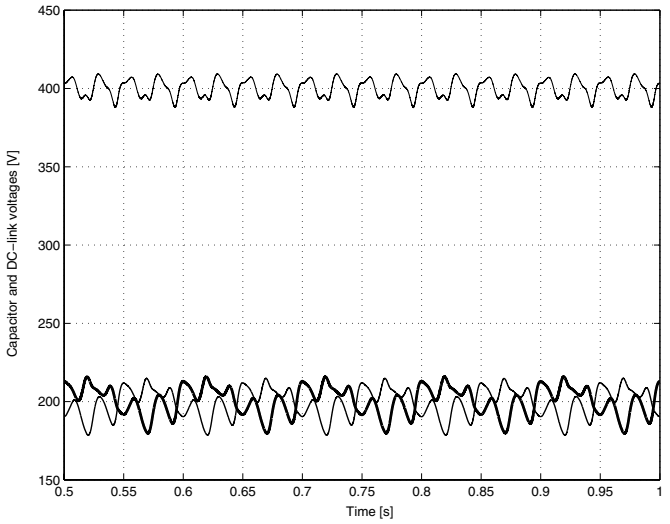

Fig. 11. DC-link and capacitor voltages: $v_{DC}(t)$ (thin line), $v_{DC1}(t)$ (medium line) and v_{DC2} (thick line).

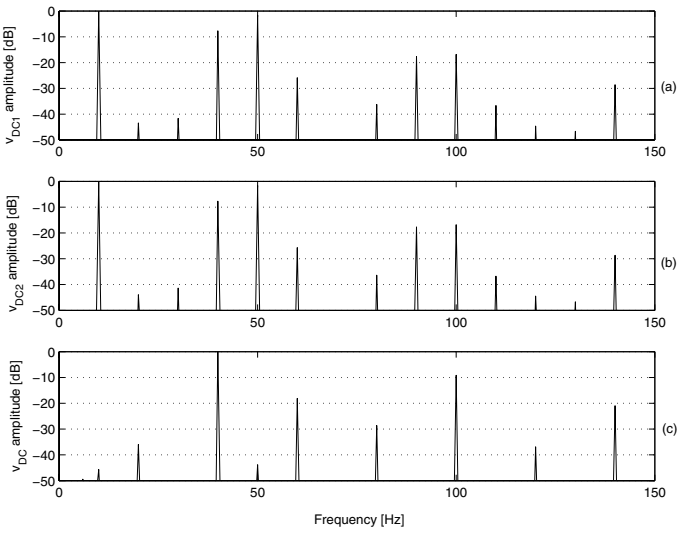

Fig. 12. Frequency spectra of capacitor and DC-link voltages: (a) $v_{DC1}(t)$, (b) $v_{DC2}(t)$, (c) $v_{DC}(t)$.

Finally, Table I resumes the number of Switches and Capacitors needed for each phase of a Multicell converter for different output voltage levels and power cell topologies. It is very interesting to note that although the H-H cell requires more semiconductors per cell, it needs the same number of switches than the Reduced cell for 3, 5 and 7 levels, but the amount of DC-link capacitors is dramatically increased with the latter.

For converters with more than 2 levels, the semireduced cell needs at most the same number of power switches than the other topologies, but requires a double amount of DC-link capacitors than the H-H cell. However, it must be noticed that the capacitors used for the semireduced cell work with half of the voltage required on the H-H cell capacitor.

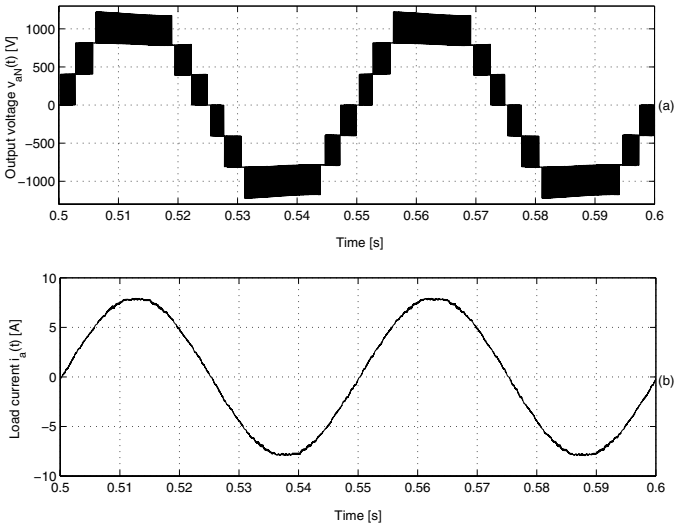

Fig. 13. Output voltage and current of the power converter working with $f_o = 20[Hz]$: (a) $v_{aN}(t)$, (b) $i_a(t)$.

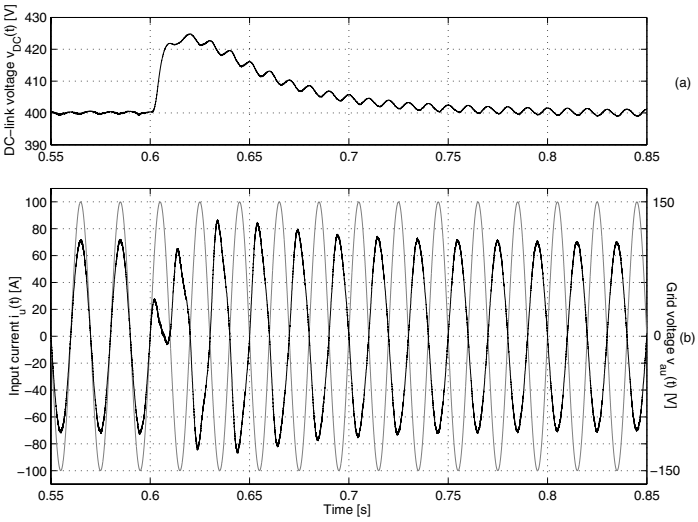

Fig. 14. Regenerative operation with $f_o = 50$[Hz]: (a) $v_{DC}(t)$, (b) $i_u(t)$ (black) and $v_{au}(t)$ (grey).

VI. Conclusions

The cell introduced in this work has a reduced number of power switches at a cost of increasing the number of DC-link capacitors, but each one working at lower voltage.

An additional advantage is that a standard industrial 6-semiconductor module, used for any conventional 2-level inverter, can be used to build the entire cell.

In addition, the control strategy for the rectifier stage keeps the balance in the voltage of the DC-link capacitors without phase-shift between the input voltage and the fundamental frequency of the input current of each cell. The low frequency input current harmonics of each cell can be effectively eliminated at the the primary side of the input transformer through a proper interconnection.

The use of a two-level single-phase PWM rectifier (Semireduced Cell) instead a three-level (H-H Bridge) can increase the high frequency ripple on the input current; this

TABLE I
NUMBER OF SWITCHES (S) AND DC-LINK CAPACITORS (C) PER NUMBER OF OUTPUT VOLTAGE LEVELS FOR CELLS WITH SINGLE-PHASE REGENERATIVE RECTIFIERS.

Output Voltage Levels	H-H Cell		Reduced Cell		Semireduced Cell	
	S	C	S	C	S	C
2	8	1	4	2	6	2
3	8	1	8	4	6	2
4	16	2	12	6	12	4
5	16	2	16	8	12	4
6	24	3	20	10	18	6
7	24	3	24	12	18	6

effect can be minimized using a proper shift between the carriers of the PWM modulators.

The authors believe that the proposed cell is a good compromise between cost and performance.

Acknowledgments

The authors acknowledge the support of the Chilean Research Fund (Fondecyt) through grant No. 1030368, the support to the post-graduate program given by Fundación Andes under grant C-14055, and of the Universidad Técnica Federico Santa María.

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